In the Claims:

Please amend claims 1-5, and add new claims 13-17 as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type having opposed first and second major surfaces;

a semiconductor component defined adjacent to the first major surface;

a trench extending from the first major surface into the semiconductor substrate, having an inner side facing the semiconductor component and an outer side opposed to the semiconductor component;

a thermal oxide filling the trench; and

an asymmetric channel stop diffusion of a second ~~first~~ conductivity type opposite to the first conductivity type, the asymmetric channel stop diffusion extending from the first major surface on the outer side of the trench and further extending under the trench from the outer side to the inner side of the trench to define an area of higher doping concentration adjacent to the outer side of the trench and an area of lower doping concentration adjacent to the inner side of the trench.

2. (Currently amended) The [[A]] semiconductor device ~~according to~~ of claim 1, further comprising a well of ~~a~~ the second conductivity type ~~opposite to the first conductivity type~~ implanted into the first major surface of the semiconductor substrate; wherein the trench extends from the first major surface through the well into the substrate.

3. (Currently amended) The [[A]] semiconductor device ~~according to~~ of claim 2, wherein the semiconductor component is a first transistor, the semiconductor device further comprising:

a second transistor adjacent to the first transistor;

a second trench ~~around~~ surrounding the second transistor extending from the first major surface into the semiconductor substrate, having an inner side facing the second transistor and an outer side opposed to the second transistor; and

a thermal oxide filling the second trench;

wherein the channel stop diffusion extends from the first major surface between the outer side of the trench and the outer side of the ~~first and~~ second trench[[es]], the channel stop diffusion further extending under ~~each of~~ the ~~first and~~ second trench[[es]] to the inner side of the second trench.

4. (Currently amended) The [[A]] semiconductor device ~~according to~~ of claim 2 [[1]], wherein the semiconductor component is an insulated gate field effect transistor having longitudinally spaced source and drain implants in the well defining a channel region at the first major surface between the source and drain implants.

5. (Currently amended) The [[A]] semiconductor device ~~according to~~ of claim 4, further comprising a gate oxide over the channel region ~~of~~ on the first major surface and a gate over the gate oxide, wherein the trench surrounds the insulated gate field effect transistor and wherein the gate oxide and the gate span the channel region from the trench on one side of the channel region to the trench on the other side of the channel region so that the channel region extends laterally between the trench[[es]].

Claims 6-12. (*Cancelled*)

13. (New) The semiconductor device of claim 4, wherein the trench surrounds the semiconductor component and the channel region extends from one side of the trench up to the other side of the trench.

14. (New) The semiconductor device of claim 1, wherein the trench is completely filled with the thermal oxide.

15. (New) The semiconductor device of claim 3, wherein the channel stop diffusion surrounds the trench and the second trench.

16. (New) The semiconductor device of claim 5, further comprising a passivation layer on the first major surface of the semiconductor substrate, the passivation layer extending over the gate, the trench, and the channel stop diffusion.

17. (New) The semiconductor device of claim 1, wherein in the trench extends approximately 2 μm from the first major surface into the semiconductor substrate and the trench has a width of approximately 1 μm.